Lasks registering with table <near> primary prod

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Method for automatically transitioning from V86 mode to protected mode in a computer system using an Intel 80386 or 80486

### processor

MD Melo - US Patent 5,255,379, 1993 - Google Patents

... and possibly a task gate descriptor) must be created and 25 placed in the global descriptor table so that ... In addition, a task register TR must be loaded with an index to the TSS descriptor in the global ... It is 30 this structure which is used for switching between the V86 mode tasks. ...

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### The anatomy of the register file in a multiscalar processor

SE Breach, TN Vijaykumar, GS Sohi - Proceedings of the 27th ..., 1994 - portal acm.org ... processor, which implies that register values must wait at the tail (until such time as the tail

advances). Accordingly, each register value propagates at most once around the ring, although most register values propagate far less, depending upon the characteristics of the tasks [5]. ...

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## Task selection for a multiscalar processor

TN Vilaykumar, GS Sohi - Proceedings of the 31st annual ACM/ ..., 1998 - portal acm.org

... The inter-task prediction uses a path-based scheme [9] with 16-bit history, 64K-entry table of 2-bit counters and 2-bit target numbers. The register communication ring can carry 2 values per cycle and bypass values in the same cycle between adjacent PUS. ...

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## Microprocessor memory management and protection mechanism

RHE Childs Jr., Jl. Klebanoff, FJ Pollack - US Patent 4,442,484, 1984 - Google Patents

... TABLE LIMIT NO 306 YES READ ACCESS RIGHTS FROM DESCRIPTOR TABLE 308 YES ... FIELD WITH VALUE OF BASE IN DESCRIPTOR 326 LOAD SEGMENT REGISTER AR FIELD ... of the

intended protection provide full multitasking, real-time executive with task, operations ...

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## Fault tolerant computer system with provision for handling external events

BJ Gleeson - US Patent 5,363,503, 1994 - Google Patents

... TABLE XH BKUP TASK 32 AND 42 AGREE MI.M2.M3.M4.M5 HAVE BEEN TRANSMITTED BKUP ... symbolic "is assigned the value" MRC - Memory Reference Counter MRCCR - Memory Reference Counter Control Register FIG ... The backup play back the failed primary task of FIG ...

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psu.edu (PDF)

### Redundant multitasking industrial controllers synchronized data tables

MA Flood - US Patent 5,912,814, 1999 - Google Patents

... that all the data has been 40 45 50 60 65 received based upon the **task** number in the ... by sequence number 8. This latter transfer transfers only changed data as indicated by flag **register** 60fc and is ... Accordingly in the event of a switch-over, the data in I/O data **table** 40fc can be ...

Cited by 6 - Related articles - All 2 versions

### Dual hardware channels and hardware context switching in a graphics rendering processor

JM Peaslee, JC Malacame - US Patent 5,371,849, 1994 - Google Patents

... 6, 1994 Sheet 7 of 7 5,371,849 7168 6175 6145 6144 Attribute register 2 Attribute register 1

—**Table** 32 —**Table** 2 —**Table** 1 FIG. ... 5,371,849 1 2 priority second channel **task**, then restoring the inter- DUAL HARDWARE CHANNELS AND rupted first channel **task**, and then ...

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### Processor-selection system

A Inoue - US Patent 4,954,945, 1990 - Google Patents

... The respective **processor** comprises a **task table** for storing the types of processable **tasks** and processes performance levels, a flag **register** for storing a flag showing that the **processor** is now being occupied, and a comparator for delivering a process-enable ...

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## Multiprocessor computer apparatus employing distributed communications paths and a passive task register

FE Heart, SM Ornstein, WB Barker, WR ... - US Patent ..., 1978 - Google Patents

... **Primary** Examiner—Melvin B. Chapnick Attorney, Agent, or Firm—Kenway & Jenney [57] ABSTRACT 3,416,139 ... 4 is a logic diagram of a passive **task register** characteristic often contributing to reliability ... bus end of such a coupler 30 listed in the following **table** together with ...

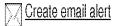
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## A design space evaluation of grid processor architectures

R Nagarajan, K Sankaralingam, D ... - 34th ACM/IEEE ..., 2001 - leeexplore leee.org

... along the shortest phys- ical path, and that banked instruction caches reside **near** the units to ... the execution: there is no centralized, associative issue window, no **register** renaming **table** and there ... Instruction group in- puts are fetched from the **register** file banks and injected from ...

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nasa.gov [PDF]

### [PDF] Near real-time parallel image processing using cluster computers

G Klimeck, F Oyafuso, M McAuley, R Deen, G Yagi, E ... - Space, 2003 - tra-new.jpl.nasa.gov ... near ... the optical correlation in the brain appears to function with incredible ease, the digital correlation of two images is a numerically intensive task. ... a multi-level test- only entry and exit from a function is computationally very expensive since it results in register push operations. ...

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## Multiprocessor computer apparatus employing distributed communications paths and a passive task register

FE Heart, SM Ornstein, WB Barker, WR ... - US Patent .... 1978 - Google Patents

... 4 is a logic diagram of a passive task register characteristic often contributing to reliability problems ... address and data on the memory bus and by loading into the control register 95, a ... other processor and, even further, can reach back up through the other **processor's** bus coupler ...

Cited by 68 - Related articles

## A scatter search-based technique for pair-wise 3D range image registration in forensic anthropology

150.214.190.154 [PDF]

J Santamaría, O Cordón, S Damas, I Alemán, M ... - Soft Computing-A ..., 2007 - Springer ... Image registration (IR) is the task that aims at find- ing the optimal point/surface correspondence/ overlap-ping ... The aim of our proposal is finding a **near**-optimal geo-metric transformation, competitive enough considering both ... 4.1 Image registration problems considered ...

Cited by 22 - Related articles - St. Direct - All 6 versions

## Balancing register allocation across threads for a multithreaded network processor

psu.edu (PDF)

X Zhuang, S Pande - Proceedings of the ACM SIGPLAN 2004 ..., 2004 - portal.acm.org ... Therefore, we should assume tasks might be different for threads on the same PU. Item 1 indicates that the registers may not be sufficient on the network **processor**. Item 2 and 3 support the feasibility of a compiler solution to optimize the **register** allocation. ...

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### Multiscalar processors

psu.edu (PDF)

GS Sohi, SE Breach, TN Vijaykumar - Proceedings of the 22nd ..., 1995 - portal.acm.org ... until all predecessor tasks have completed all stores, with the likely outcome being near-sequential execution ... The release of a register may be indicated by adding a special re/ease Instruction ... A pictorial representation of the information assem-bled within a task of a multiscalar ...

Cited by 844 - Related articles - BL Direct - All 64 versions

## ProteomeGRID: towards a high-throughput proteomics pipeline through opportunistic cluster image computing for twodimensional gel electrophoresis

AW Dowsey, MJ Dunn, GZ Yang - Proteomics, 2004 - Interscience wiley.com

... ProteomeGRID cluster image computing 3809 Figure 6. (a) Multiresolution image registration using **near**-lossless JPEG-LS ... (b) Make-span of the 60 gel **pair**-wise registra- tion experiment (3540 tasks), performed by cluster computing with worker groups between 5 and 40. ...

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### A level-set based approach to image **registration**

kent.edu (PDF)

BC Vemuri, J. Ye, Y. Chen, CM ... - IEEE Workshop on ..., 2000 - ieeexplore.ieee.org ... The image registration problem can be formulated as a motion estimation task, more specifically the es ... measure are currently being investigated and the results would be availablein the near future. ... how ev er a little noisy and not as accurate as the results of registration from the ... Cited by 41 - Related articles - All 7 versions

## A near-exact method for solving the log-truck scheduling problem

M Palmgren, M Rönngvist, P ... . ... in Operational Research, 2004 - interscience wiley.com ... a time. It proceeds dynamically during the day until all tasks have been covered. The advantage ... and price. For this reason the method is referred to as **near**-exact. The paper ... of iterations. At this time we **register** the lower bound. Given an ...

Cited by 15 - Related articles - BL Direct - All 5 versions

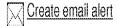
# Multiprocessor system shaving processor based idle state detection and method of executing tasks in such a multiprocessor system

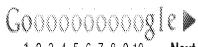
T Tanaka, A Fukuda, H Tanuma - US Patent 5,867,704, 1999 - Google Patents

... 9 Processor Task IDLE Idle RUN Run STOP Waiting to be executed or having been executed EX1 ... 12 Task management device TaskO) CTaskn (Task2) (Task3) (Task4 Register task waiting to be executed (^rocessoriT) (TrocessorT) (^Processor?) Processor assignment FIG. ... Otted by 4 - Related articles

## 3D Forensic Model Reconstruction by Scatter Search-based Pair-wise Image Registration

J Santamaría, O Cordón, S Damas, I Alemán, ... - ... Conference on Fuzzy ... - leeexplore.leee.org ... also to provide a more robust and more accurate technique than those in the IR literature for forensic anthropology tasks. ... The aim of our proposal is finding a near-optimal geo- metric transformation, competitive enough considering both ... 2. Pair-wise image registration framework ... Cited by 3 - Related articles





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